

CLAIMS

Having thus described our invention in detail, what we claim is new and desire to secure by the Letters Patent is:

1 1. A method of reducing the dislocations present in a SiGe heterojunction bipolar
2 transistor, said method comprising the steps of:
3
4 (a) providing a semiconductor substrate having isolation regions formed therein, said
5 semiconductor substrate having an upper surface;
6
7 (b) recessing a portion of the isolation regions below the upper surface of said
8 semiconductor substrate so as to provide a recessed isolation surface; and
9
10 (c) forming a SiGe layer on the upper surface of the semiconductor substrate as well as
11 said recessed isolation surface, wherein said recessing controls facet formation at edges
12 of the SiGe layer.

1 2. The method of Claim 1 wherein said isolation regions are trench isolation regions.

1 3. The method of Claim 2 wherein said trench isolation regions are formed by
2 lithography, etching and trench filling.

1 4. The method of Claim 3 wherein said trench filling includes deposition of SiO₂.

1 5. The method of Claim 1 wherein a patterned dielectric layer is formed on a portion of
2 said isolation regions prior to conducting step (b).

1 6. The method of Claim 5 wherein said dielectric is composed of a nitride.

1 7. The method of Claim 1 wherein said recessing includes lithography and etching.

1 8. The method of Claim 1 wherein after said recessing a patterned dielectric is formed
2 on a portion of the isolation region that is not recessed.

1 9. The method of Claim 1 wherein said SiGe layer is formed by a deposition process
2 selected from the group consisting of ultra-high vacuum chemical vapor deposition
3 (UHVCVD), molecular beam epitaxy (MBE), rapid thermal chemical vapor deposition
4 (RTCVD) and plasma-enhanced chemical vapor deposition (PECVD).

1 10. The method of Claim 1 further comprising the steps of:
2

3 (d) forming an insulator on said SiGe layer;
4

5 (e) providing an opening in said insulator so as to expose a portion of said SiGe base
6 region;
7

8 (f) forming an emitter material on said insulator and in said opening so as to contact said
9 SiGe base region; and
10

11 (g) patterning said emitter material and said insulator so as to form a patterned emitter
12 and a patterned insulator on said SiGe base region.

1 11. A SiGe bipolar transistor comprises:

2 a semiconductor substrate having a collector and sub-collector formed therein, wherein
3 said collector is formed between isolation regions that are also present in the substrate,
4 each of said isolation regions having a recessed surface and a non-recessed surface;
5

6 a SiGe layer formed on said substrate as well as said recessed and non-recessed surfaces
7 of each isolation region, said SiGe layer including polycrystalline Si regions and a SiGe
8 base region;
9

10 a patterned insulator layer formed on said SiGe base region, said patterned insulator
11 layer having an opening therein; and
12

13 an emitter formed on said patterned insulator layer and in contact with said SiGe base
14 region through said opening.

1 12. The SiGe bipolar transistor Claim 11 wherein said non-recessed surface includes a
2 dielectric material formed thereon.

- 1 13. The SiGe bipolar transistor of Claim 12 wherein said dielectric material is a nitride.
- 1 14. The SiGe bipolar transistor of Claim 11 wherein said semiconductor substrate is
2 composed of a semiconducting material selected from the group consisting of Si, Ge,
3 SiGe, GaAs, InAs, InP, Si/Si and Si/SiGe.
- 1 15. The SiGe bipolar transistor of Claim 14 wherein said semiconducting material is Si.
- 1 16. The SiGe bipolar transistor of Claim 11 wherein said isolation regions are trench
2 isolation regions.
- 1 17. The SiGe bipolar transistor of Claim 11 wherein said isolation regions are filled
2 with SiO₂.
- 1 18. The SiGe bipolar transistor of Claim 11 wherein said patterned insulator is
2 composed of an oxide, a nitride, an oxynitride or any combination thereof.
- 1 19. The SiGe bipolar transistor of Claim 11 wherein said emitter is composed of doped
2 polysilicon.